IN THE CLAIMS

1. (Currently amended) A filter, comprising:

a tap multiplication circuit that receives sample decisions and equalization coefficients;

a tap digital-to-analog ("DAC") unit coupled to the tap multiplication circuit; and

a plurality of clocks that control timing associated with the tap multiplication circuit and that permit one tap multiplication to be output while another tap multiplication is being computed;

wherein said tap multiplication circuit comprises a plurality of tap multiplication units, each tap multiplication unit comprising a first transistor that is controlled to output a tap coefficient current, and a second transistor that is controlled to provide current through a conducting branch that is separate from a branch in which the tap coefficient current is output, wherein the first transistor and the second transistor [[are]] do not [[on]] provide current at the same time.

2. (Original) The filter of claim 1 wherein the tap DAC unit comprises a break-before-make switch that, when a coefficient bit transitions logic states, precludes a gate of a current source from being grounded and then couples the gate to a control voltage.

3. (Original) The filter of claim 1 further comprising a replica bias circuit coupled to the tap multiplication circuit and the DAC unit, the replica bias circuit provides substantially constant DAC steps regardless of variations in voltage associated with a current source in the tap DAC unit.

4 and 5. (Cancelled)

6. (Currently amended)A communication apparatus, comprising:

a summer;

a slicer coupled the summer and that generates sample decisions; and

a filter coupled to the slice and the summer that receives equalization coefficients and sample decisions and generates and provides an equalization signal to the summer, the filter comprising a tap multiplication circuit, a tap digital-to-analog ("DAC")

unit coupled to the tap multiplication circuit, and a plurality of clocks that control timing associated with the tap multiplication circuit and that permit one tap coefficient to be output while another tap coefficient is being computed.

wherein said tap multiplication circuit in the filter comprises a plurality of tap multiplication units, each tap multiplication unit comprising a first transistor that is controlled to output a tap coefficient current, and a second transistor that is controlled to provide current through a conducting branch that is separate from a branch in which the tap coefficient current is output, wherein the first transistor and the second transistor [[are]] do not [[on]] provide current at the same time.

7. (Original) The apparatus of claim 6 wherein the tap DAC unit comprises a break-before-make switch that, when a coefficient bit transitions logic states, precludes a gate of a current source from being grounded and then couples the gate to a control voltage.

8. (Original) The apparatus of claim 6 further comprising a replica bias circuit coupled to the tap multiplication circuit and the DAC unit, the replica bias circuit provides substantially constant DAC steps regardless of variations in voltage associated with a current source in the tap DAC unit.

9-11. (Withdrawn)